What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A programmable circuit comprising:

a programmable transistor which is selectively programmable to have its gate threshold voltage at one of a first gate threshold voltage and a second threshold voltage; and

a read circuit for reading the program status of said programmable transistor, said circuit applying voltage to source and drain terminals of said programmable transistor and a third threshold voltage which is between said first and second threshold voltages to a gate of said programmable transistor, said read circuit determining the operative state of said programmable transistor when said third threshold voltage is applied.

2. A programmable circuit as in claim 1 wherein said read circuit comprises:

a first circuit portion for applying said third threshold voltage to said gate during a read operation; and

a second circuit portion for determining the operative status of said transistor during said read operation.

3. A programmable circuit as in claim 2 wherein said second circuit portion includes a latch having an input node coupled to one of a source and drain terminal of said transistor, the operative state of said transistor determining the voltage at said input node and controlling the output state of said latch at an output node during said read operation.

4. A programmable circuit as in claim 3 wherein said latch comprises an inverter having an input coupled to said input node and an output coupled to said output node.

5. A programmable circuit as in claim 3 wherein said latch circuit comprises:

an input node for receiving a read signal which renders said latch operative to determine the voltage at said input node.

6. A programmable circuit as in claim 5 wherein said latch circuit further comprises:

a first and a second transistor, each having a source and drain terminal, said first and second transistors having their source and drain terminal connected in parallel, said first and second transistors being connected between a first potential source and said latch input node;

a third and a fourth transistor, each having a source and drain terminal, said third and fourth transistors having their source and drain terminals serially connected, said third and fourth transistors being serially connected between said latch input node and a second potential source;

the gates of said second and fourth transistors being coupled to said output node of said latch and the gates of said first and third transistors being coupled to said read signal line.

7. A programmable circuit as in claim 6 wherein said first and second transistors are p-channel transistors and said third and fourth transistors are n-channel transistors.

8. A programmable circuit as in claim 6 wherein said first and second transistors are coupled to said first potential through a fifth transistor, the gate of said fifth transistor being coupled to a signal line which receives a control signal to control the supply of power from said first power source to said latch circuit.

9. A programmable circuit as in claim 8 further comprising a signal generator for generating said control signal at least during said read operation.

10. A programmable circuit as in claim 1 further comprising:

a programming circuit for programming said programmable transistor by applying predetermined voltages to terminals of said programmable transistor to change said gate threshold voltage from one of said first and second gate threshold voltages to the other of said first and second gate threshold voltages.

11. A programmable circuit as in claim 10 wherein said programming circuit applies said predetermined voltages to a gate and drain terminals of said programmable transistor.

12. A programmable circuit as in claim 11 wherein said programmable transistor is an n-channel transistor.

13. A programmable circuit as in claim 1 further comprising:

a read signal generator for generating a read signal, said read circuit being responsive to said read signal for determining the operative state of said programmable transistor.

14. A programmable circuit as in claim 6 further comprising:

a read signal generator for generating a read signal on said read signal line.

15. A programmable circuit as in claim 3 wherein a source at said programmable transistor is coupled to said input node, and a drain of said programmable transistor is coupled to a voltage potential when said third threshold voltage is applied to said gate terminal.

16. A programmable circuit as in claim 1 wherein said programmable circuit is provided in an integrated circuit.

17. A programmable circuit as in claim 1 wherein said integrated circuit is a memory device.

18. A memory device comprising:

a programmable transistor which is selectively programmable to have its gate threshold voltage at one of a first gate threshold voltage and a second threshold voltage; and

a read circuit for reading the program status of said programmable transistor, said circuit applying voltage to source and drain terminals of said programmable transistor and a third threshold voltage which is between said first and second threshold voltages to a gate of said programmable transistor, said read circuit determining the operative state of said programmable transistor when said third threshold voltage is applied.

19. A memory device as in claim 18 wherein said read circuit comprises:

a first circuit portion for applying said third threshold voltage to said gate during a read operation; and

a second circuit portion for determining the operative status of said transistor during said read operation.

20. A memory device as in claim 19 wherein said second circuit portion includes a latch having an input node coupled to one of a source and drain terminal of said transistor, the operative state of said transistor determining the voltage at said input node and controlling the output state of said latch at an output node during said read operation.

21. A memory device as in claim 20 wherein said latch comprises an inverter having an input coupled to said input node and an output coupled to said output node.

22. A memory device as in claim 20 wherein said latch circuit comprises:

an input node for receiving a read signal which renders said latch operative to determine the voltage at said input node.

23. A memory device as in claim 22 wherein said latch circuit further comprises:

a first and a second transistor, each having a source and drain terminal, said first and second transistors having their source and drain terminal connected in parallel, said first and second transistors being connected between a first potential source and said latch input node;

a third and a fourth transistor, each having a source and drain terminal, said third and fourth transistors having their source and drain terminals serially connected, said third and fourth transistors being serially connected between said latch input node and a second potential source;

the gates of said second and fourth transistors being coupled to said output node of said latch and the gates of said first and third transistors being coupled to said read signal line.

24. A memory device as in claim 23 wherein said first and second transistors are p-channel transistors and said third and fourth transistors are n-channel transistors.

25. A memory device as in claim 23 wherein said first and second transistors are coupled to said first potential through a fifth transistor, the gate of said fifth transistor being coupled to a signal line

which receives a control signal to control the supply of power from said first power source to said latch circuit.

26. A memory device as in claim 25 further comprising a signal generator for generating said control signal at least during said read operation.

27. A memory device as in claim 18 further comprising:

a programming circuit for programming said programmable transistor by applying predetermined voltages to terminals of said programmable transistor to change said gate threshold voltage from one of said first and second gate threshold voltages to the other of said first and second gate threshold voltages.

28 . A memory device as in claim 27 wherein said programming circuit applies said predetermined voltages to a gate and drain terminals of said programmable transistor.

29. A memory device as in claim 28 wherein said programmable transistor is an n-channel transistor.

30. A memory device as in claim 18 further comprising:

a read signal generator for generating a read signal, said read circuit being responsive to said read signal for determining the operative state of said programmable transistor.

31. A memory device as in claim 23 further comprising:

a read signal generator for generating a read signal on said read signal line.

32. A memory device as in claim 20 wherein a source at said programmable transistor is coupled to said input node, and a drain of said programmable transistor is coupled to a voltage potential when said third threshold voltage is applied to said gate terminal.

33. A processor system comprising:

a processor; and

at least one memory device coupled to said processor, at least one of said memory device and processor comprising a programmable circuit, said programmable circuit comprising:

a programmable transistor which is selectively programmable to have its gate threshold voltage at one of a first gate threshold voltage and a second threshold voltage; and

a read circuit for reading the program status of said programmable transistor, said circuit applying voltage to source and drain terminals of said programmable transistor and a third threshold voltage which is between said first and second threshold voltages to a gate of said programmable transistor, said read circuit determining the operative state of said programmable transistor when said third threshold voltage is applied.

34. A system as in claim 33 wherein said read circuit comprises:

a first circuit portion for applying said third threshold voltage to said gate during a read operation; and

a second circuit portion for determining the operative status of said transistor during said read operation.

35. A system as in claim 34 wherein said second circuit portion includes a latch having an input node coupled to one of a source and drain

terminal of said transistor, the operative state of said transistor determining the voltage at said input node and controlling the output state of said latch at an output node during said read operation.

36. A system as in claim 35 wherein said latch comprises an inverter having an input coupled to said input node and an output coupled to said output node.

37. A system as in claim 35 wherein said latch circuit comprises:

an input node for receiving a read signal which renders said latch operative to determine the voltage at said input node.

38. A system as in claim 37 wherein said latch circuit further comprises:

a first and a second transistor, each having a source and drain terminal, said first and second transistors having their source and drain terminal connected in parallel, said first and second transistors being connected between a first potential source and said latch input node;

a third and a fourth transistor, each having a source and drain terminal, said third and fourth transistors having their source and drain

terminals serially connected, said third and fourth transistors being serially connected between said latch input node and a second potential source;

the gates of said second and fourth transistors being coupled to said output node of said latch and the gates of said first and third transistors being coupled o said read signal line.

39. A system as in claim 38 wherein said first and second transistors are p-channel transistors and said third and fourth transistors are n-channel transistors.

40. A system as in claim 38 wherein said first and second transistors are coupled to said first potential through a fifth transistor, the gate of said fifth transistor being coupled to a signal line which receives a control signal to control the supply of power from said first power source to said latch circuit.

41. A system as in claim 40 further comprising a signal generator for generating said control signal at least during said read operation.

42. A system as in claim 33 further comprising:

a programming circuit for programming said programmable transistor by applying predetermined voltages to terminals of said programmable transistor to change said gate threshold voltage from one of said first and second gate threshold voltages to the other of said first and second gate threshold voltages.

43. A system as in claim 42 wherein said programming circuit applies said predetermined voltages to a gate and drain terminals of said programmable transistor.

44. A system as in claim 43 wherein said programmable transistor is an n-channel transistor.

45. A system as in claim 33 further comprising:

a read signal generator for generating a read signal, said read circuit being responsive to said read signal for determining the operative state of said programmable transistor.

46. A system as in claim 38 further comprising:

a read signal generator for generating a read signal on said read signal line.

47. A system as in claim 33 wherein a source at said programmable transistor is coupled to said input node, and a drain of said programmable transistor is coupled to a voltage potential when said third threshold voltage is applied to said gate terminal.

48. A method of operating a programmable circuit, said method comprising:

causing a gate threshold voltage level of a programmable transistor to be at one of a first gate threshold voltage value and a second gate threshold voltage value; and

determining an operative state of said programmable transistor during a time when said transistor is biased for operation and a third gate threshold voltage, between said first and second threshold voltage values, is applied to a gate of said programmable transistor when said third threshold voltage is applied.

49. A method as in claim 48 wherein said determining further comprises driving a latch to a predetermined operative state in accordance with the operative state of said programmable transistor.

50. A method as in claim 48 wherein said determining step occurs in response to the occurrence of a read signal.

51. A method as in claim 49 wherein said determining step occurs in response to the occurrence of a read signal.

52. A method as in claim 51 further comprising selectively rendering said latch operative to determine an operative state of said programmable transistor in response to said read signal.

53. A method as in claim 48 wherein said causing includes programming said programmable transistor by applying predetermined voltages to terminals of said programmable transistor to change said gate threshold voltage from one of said first and second gate threshold voltages to the other of said first and second gate threshold voltages.

54. A method as in claim 54 wherein said predetermined voltages are applied to gate and drain terminals of said programmable transistor.

55. A method of operating a programmable circuit comprising:

causing the gate threshold voltage of a programmable transistor to move from one of a first gate threshold voltage and a second gate threshold voltage to the other of said first gate threshold voltage and said second gate threshold voltage by applying predetermined voltages to a gate and drain terminal of said programmable transistor.